|  |
| --- |
|  |
| **Interface Control Document**  Systems Engineering**-Company E** |
| **COP** |
| Prepared for: |
| Anders Jacob Truelsen (Systematic)  By: Anders Torndahl, Christian Jensen, David Neergaard Rasmussen Marmoy, Michael Nygaard Pedersen, Peter Høgh Mikkelsen |
|  |
|  |

|  |  |
| --- | --- |
|  | |
| System requirement specification | |
| Project: | $System Engineering**– Company E** |
| Revision: | $Revision: 1A$ $Date:08102010$ |
| Document: | $ |
| Copyright (c) 2010 by Systematic Group. It shall not be copied, reproduced, disclosed or otherwise made available to third party without previous consent from Systematic Group | |

Table of Contents

[1 Introduction 1](#_Toc274146111)

[2 Interface design 1](#_Toc274146112)

[2.1 Interface identification and diagrams 1](#_Toc274146113)

[2.2 CCRT and CCRC Interface 2](#_Toc274146114)

[2.2.1 Type of interface 2](#_Toc274146115)

[2.2.2 Interface data elements and setup 3](#_Toc274146116)

[2.2.3 Address bus 3](#_Toc274146117)

[2.2.4 Data bus 3](#_Toc274146118)

[2.2.5 Memory Map 3](#_Toc274146119)

[2.2.6 Control registers 3](#_Toc274146120)

[2.2.7 Status registers 3](#_Toc274146121)

[2.2.8 Data registers 3](#_Toc274146122)

[2.2.9 Hardware characteristics 3](#_Toc274146123)

[3 Bibliography 4](#_Toc274146124)

# Introduction

This document describes the analysis process on the case work with the Common Operations Picture (COP) case from Systematic. Company E is the main contractor and this document will explain one of the critical interfaces involved.

# Interface design

This paragraph describes the interface characteristics of one block within the COP domain.

It is recommended to read the System Requirement Specification before reading this document.

points-out the chosen block, where this interface control document will focus, and leave other interfaces as unexplored interfaces.



Figure 1 - SysML block diagram

## Interface identification and diagrams

This paragraph contains an identification of the limited system, which has been chosen to be described during this case work.

Figure 2, shows the chosen system interfaces.



Figure 2 - System interfaces

1. CCRT (Cross compatible radio - terminals): The interface between the different branches involved.
2. CCRC (Cross compatible radio - control): The interface to the headquarter, which provides and maintain the infrastructure and technology of this solution.

shows the overall setup of the interfaces.

|  |  |  |  |
| --- | --- | --- | --- |
| **Channel name** | **Source** | **Sink** | **Channel frequency** |
| CCRT | Bi-directional | | 380 - 921 MHz |
| CCRC | Bi-directional | | 380 - 921 MHz |

Table 1 - Interface overview

## CCRT and CCRC Interface

These two interfaces are treated as identical in this document since they, from a interface architects point-of-view, could be described the same way.

CCRT and CCRC will use the SINE solution , which is based TETRA technology, which is a wireless standard. TETRA is designed for use by government agencies, emergency services, police forces, fire departments, ambulance, rail transportation staff, and transport services.

TETRA is an ETSI standard [4] and works in a very similar way to GSM. The main differences are longer range and more bandwidth allocated for data.

### Type of interface

This interface complies with the TETRA communication standard [2]. It is a data transceiver interface, which will send or receive non-buffered data packages from the respective unit.

### Interface data elements and setup

The TETRA system is a Frequency Division Duplex (FDD) system. TETRA also uses FDMA/TDMA like GSM.

Modulation setup [3]:

* Digital modulation scheme: π/4 DQPSK (differential quadrature phase shift keying)
* Baud rate: 18000 sym/s
* Symbol maps: 2 bits/sym

Speech signals are the essential part of TETRA technology.

Speech channel [3]:

* Sampled at: 8 kbit/s
* Compressed with: ACELP (Adaptive Code Excited Linear Prediction).
* Data rate before channel coding: 4,567 kbit/s.
* Data rate after channel coding: 7,2 kbit/s.

A single slot consists of 255 usable symbols, the remaining time is used up with synchronisation sequences and turning on/off

### Address bus

NA

### Data bus

NA

### Memory Map

NA - Not a memory mapped interface

### Control registers

Read the TETRA ETSI standard [4]

### Status registers

Read the TETRA ETSI standard [4]

### Data registers

Read the TETRA ETSI standard [4]

### Hardware characteristics

Read the TETRA ETSI standard [4]

# Bibliography

1. **sikkerhedsnet.dk**.SINE-sekretariate, 2010.
2. **tetra-association.com**. The TETRA MoU Association Ltd, 2010.
3. **En.wikipedia.org/wiki/Terrestrial\_Trunked\_Radio**, Wikipedia, 2010
4. **etsi.org/website/Technologies/TETRA.aspx**. ETSI, 2010