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| **Interface Control Document**  Systems Engineering**-Company E** |
| **COP** |
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| System requirement specification | |
| Project: | $System Engineering**– Company E** |
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# Introduction

This document describes the analysis process on the case work with the Common Operations Picture (COP) case from Systematic. Company E is the main contractor and the document includes requirements both for the main and sub contractor. The processes used are based on approaches in the INCOSE Systems Engineering Handbook[1].

First introductory sections describing the vision and scope of the project and an analysis of the stakeholder needs are presented. Then follows a section describing the requirements for the main contractor followed by a section describing sub-contractor requirements.

# Interface design

This paragraph describes the external interface characteristics of the ARINC 429 VHDL Core.

It is recommended to read the requirements to the external interfaces as described in the Requirement Specification <IRef3> before reading this document.

## Interface identification and diagrams

This paragraph contains a full identification of the system, the interfacing entities with all interfaces given a project unique identification name.

Figure 5‑1, shows a system block diagram where the interfaces of the ARINC 429 VHDL Core are in presented. The external interfaces; APLB, ALDB and ALRB is presented in this document, the internal interfaces are designed in System Design Description <IRef1>



Figure ‑: System interface block diagram

1. APLB (ARINC Processor Local Bus): This bus exchanges data between the ARINC 429 VHDL Core and the On-Chip CPU.
2. ALDB (ARINC Line Driver Bus): This bus transmits ARINC 429 compatible data words
3. ALRB (ARINC Line Receiver Bus): This bus can receive up to 8 ARINC 429 data words simultaneously

Table ‑: Interface overview

|  |  |  |  |
| --- | --- | --- | --- |
| **Channel name** | **Source** | **Sink** | **Channel frequency** |
| APLB | Bi-directional | | PLB clock (75 Mhz) |
| ALDB | ARINC 429 VHDL Core | ARINC 429 Line Driver | 100kHz/12.5kHz |
| ALRB | ARINC 429 Line Receiver | ARINC 429 VHDL Core | 100kHz/12.5kHz |

## ??? Interface

This interface will exchange data between the on-chip CPU and the ARINC 429 VHDL Core.

### Type of interface

This interface used is the PLB v46. For general information see Product Specification for PLBv46 <ERef3>.

This interface is a memory mapped interface, a memory map of the ARINC 429 VHDL Core Base Address offsets is found in Table 5‑2.

### Interface data elements and entities

When the ARINC 429 VHDL Core communicates with the On-Chip CPU, two busses are used, an address bus and a data bus, which are briefly explained below. Furthermore, the ARINC 429 VHDL Core can interrupt the On-Chip CPU.

### Address bus

The address bus has a width of 32 bits.

See Table 5‑2 for applicable memory map of the system.

### Data bus

The data bus has a bus width of 32 bit.

### Memory Map

### Control registers

### Status registers

### Data registers

The data register, contains 32-bit data words received from an ARINC 429 compatible device. Data in the registers is mirrored like explained earlier. For each input, a register is attached.

### Hardware characteristics

ARINC 429 is a two-wire data bus that uses bipolar return-to-zero modulation with three ARINC 429 logic states, “LOW”, “HIGH” and “NULL”. The truth table, Table 5‑3, specifies the hardware characteristic of the two-wire ALDB interface. (L = Logic Low, H = Logic High).

Table ‑: Truth table for ALDB

|  |  |  |
| --- | --- | --- |
| **ARINC 429 Logic** | **OUTA** | **OUTB** |
| “LOW” | L | H |
| “HIGH” | H | L |
| “NULL” | L | L |

# Bibliography

1. **International Council on Systems Engineering**.*INCOSE Systems Engineering Handbook v. 3.2a*.INCOSE, 2010.
2. **Project plan**. Company E, 2010.
3. **Requirements Traceability Matrix**, Company E, 2010